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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/921,375
Filing Date: August 02, 2001
Appellant(s): WHITNEY, RAY

John D. Gugliotta
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/03/2008 appealing from the Office action mailed 07/31/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,915,020	Tilford et al.	6-1999
6,141,062	Hall et al.	10-2000

5,428,671 Dykes et al. 6-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,915,020 (Tilford et al., hereinafter Tilford) in further view of U.S. Patent 6,141,062 (Hall et al., hereinafter Hall) and U.S. Patent 5,428,671 (Dykes et al., hereinafter Dykes).

Regarding claim 12, Tilford discloses the claimed:

a digital wireless PC/PCS modem having an antenna attached to a PCMCIA card-type interface in communication with an integrated circuit board, said modem works in conjunction with a computer (i.e., PCMCIA card having an antenna and circuitry that effects cellular communication functions, Col. 7 Line 45 – Col. 8 Line 10) provided with a swivel-based camera (i.e., small video camera, Fig. 8 Element 123, Col. 3 Lines 45-67 & Col. 13 Lines 51-57), a microphone (Fig. 8 Element 121, Col. 3 Lines 51-54 & Col 13 Lines 51-57) and [at least three] tuner cards (video decoder, Fig. 7

Element 74, Col. 7 Lines 18-25) to relay wireless communications via satellite (i.e., digital satellite system, Fig. 1 Element 20, Col. 4 Line 56 – Col. 5 Line 19).

Furthermore, Tilford discloses the claimed steps of:

passing the digital signals transmitted via a satellite link and a wireless relay system (i.e., digital satellite system, Fig. 1 Element 20, Col. 4 Line 56 – Col. 5 Line 19) from said antenna that receives said signals (i.e., antenna, Fig. 11, Col. 7 Lines 45-49) to a series of line amplifiers (i.e., amplifier, Col. 6 Lines 26-29), said series of line amplifiers and a network switching element (i.e., transport IC, Fig. 12 Element 68, Col. 11 Lines 59-61) have an input buffer (i.e., buffer, Col. 11 Lines 65-67) coupled therebetween, said network switching element receives input from said PC/PCS modem (Col. 11 Lines 41-61), said network switching element has a frequency/feedback (i.e., Feed LNB, Fig. 7 Element 41) along with a channel/screen selection function (i.e., application programs may be run simultaneously with the display of the video image, Col. 9 Lines 57-65) flowing from said switching network bi-directionally to a multi-tuner (i.e., transport IC, Fig. 7 Element 68);

passing the data received from said multi-tuner module to a microprocessor (i.e., microprocessor & transport IC, Fig. 7 Elements 65 and 68).

What Tilford does not explicitly disclose is the claimed *at least three* tuner cards and further does not explicitly disclose the steps of:

passing said data on to a universal asynchronous receiver transmitter via a first bi-directional path, said universal asynchronous receiver transmitter is responsible for all data transfers from a computer system to the computer system's output system,

wherein said data transfer occurs between all modules through a series of parallel bus, a series of serial transmit bus and a series of serial receive bus.

Regarding the claimed at least three tuner cards, Hall does disclose the claimed at least three tuner cards (i.e., video decoder, Fig. 1 Elements 220, 240 & 260, Col. 2 Lines 62-67).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to implement the feature of Hall with the combined system of Tilford and Dykes because the feature of using three tuner cards is old and well known in the prior art. The motivation to make the combination is to beneficially allow a user to access a plurality of data from multiple sources.

Regarding the claimed steps of passing said data on to a universal asynchronous receiver transmitter via a first bi-directional path, said universal asynchronous receiver transmitter is responsible for all data transfers from a computer system to the computer system's output system, wherein said data transfer occurs between all modules through a series of parallel bus, a series of serial transmit bus and a series of serial receive bus, Dykes does disclose the claimed passing said data on to a universal asynchronous receiver transmitter via a first bi-directional path, said universal asynchronous receiver

transmitter is responsible for all data transfers from a computer system to the computer system's output system (i.e., UART Support, Fig. 2 Element 100, Col. 6 Line 51 – Col. 8 Line 63), wherein said data transfer occurs between all modules through a series of parallel bus, a series of serial transmit bus and a series of serial receive bus (i.e., parallel bus, serial RX & serial TX, Fig. 2).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to implement the features of Dykes with the combined system of Tilford and Hall because the features of a universal asynchronous receiver transmitter, a series of parallel bus, a series of serial transmit bus and a series of serial receive bus is old and well known in the prior art. The motivation to implement the said features is to provide an efficient means to transmitting and receiving the data from the wireless system to the wireless PCMCIA modem.

Claim 13 is met by the combination of Tilford, Hall and Dykes, wherein Dykes discloses the claimed:

aligning said data in a proper configuration by means of a micro controller (Fig. 2 Element 102);

processing said proper configuration by means of a voice, a data, a fax and a video processor (i.e., DSP Support, DSP & Codec, Fig. 2 Elements 106, 108 & 110) through a second parallel bus, a second serial transmit bus and a second serial receive bus (i.e., parallel bus, serial RX & serial TX, Fig. 2), said voice, data, fax and video processor includes a digital signal processing support module used as a prebuffer (i.e.,

DSP Support, Fig. 2 Element 106) into a digital signal processor (i.e., DSP, Fig. 2 Element 108), and wherein said digital signal processor performs all necessary operations on said data, including handshake verification, through a series of built-in algorithms (Fig. 2, Col. 6 Line 51 – Col. 8 Line 63, the microcontroller inherently aligns data in the proper configuration to be processed by voice, data, fax, and a video processor, and the DSP inherently performs all necessary operations on the data, including handshaking verification, through a series of built in algorithms in order to communicate to the modem).

(10) Response to Arguments

Appellant argues “Tilford shows the camera fixed…[Appellant] rather claims a swivel feature to the camera." (Appellant’s Argument, Page 11)	Tilford discloses a portable device which includes a video camera (Col. 3 Lines Line 53). Examiner contends the portable device in which the video camera is enclosed is movable and therefore is understood to have the claimed "swivel" capability. Since the camera is within the enclosure, it is understood Tilford discloses the claimed swivel-based camera.
Appellants argues that "[Appellant] alternatively claims an input *buffer coupled*	The rejection is based upon Tilford in view of Hall and Dykes. Though Tilford alone

between a series of amplifiers and a network switching element." (Appellant's Argument, Page 11)	does not disclose the claimed series of amplifiers, it is understood Tilford in view of Halls and Dykes does. The combination of Tilford and Dykes in view of Hall reveals it would have been obvious to one with ordinary skill in the art at the time the invention was made to implement multiple tuner cards in a computer. Taking into account this combination, it should be understood that Tilford discloses a single amplifier in connection to a video decoder (Fig. 7, Elements 41 Feed LNB & Element 74 Video decoder, one amplifier associated for every one video decoder). Since Hall clearly discloses multiple video decoders (Fig. 1 Elements 220, 240 & 260, Col. 2 Lines 62-67) and it would have been obvious to one with ordinary skill in the art at the time the invention was made to implement the features of Hall with the

	combined system of Tilford and Dykes, it should be further understood multiple amplifiers is necessary to account for the multiple video decoders and therefore it is understood the combination of Tilford, Dykes and Hall discloses the claimed series of line amplifiers.
Appellant argues “Tilford teaches a buffer within a transport IC...[Appellant] alternatively claims an input buffer coupled between a series of amplifiers and a network switching element. Nowhere in Tilford is a buffer taught or suggested either coupled to or between the Feed LNB 41 and the tuner/modulator 62." (Appellant’s Argument, Pages 11 and 12)	It is understood the flow of the signal as disclosed in Tilford is one in which the signal travels through the amplifier, to the buffer and hence to the transport IC (since the buffer is within the transport IC). The buffer of Tilford is within the transport IC wherein the signal that comes from the amplifier is buffered before the transport IC further transmits the signal (Tilford, Col. 11 Line 65 - Col. 12 Line 7). Since the signal is being buffered before being transmitted from the transport IC it is understood Tilford discloses the claimed “receiv[ing] said signals to a series of line amplifiers, said series of line amplifiers and a network

	switching element have an input buffer coupled therebetween."

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/My X Nguyen/

Examiner, Art Unit 2617

Conferees:

/George Eng/

Supervisory Patent Examiner, Art Unit 2617

/Duc Nguyen/

Supervisory Patent Examiner, Art Unit 2617